

Search History

STN
(HCAPLUS, INSPEC, JAPIO, WPPATALL)
2/9/05

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(FILE 'HOME' ENTERED AT 08:41:15 ON 09 FEB 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 08:41:29 ON 09 FEB 2005

L1 56301 S (GAN OR GALLIUM(W)NITRIDE)
L2 566 S (NITRIDE) (8A) (SEMICONDUCTOR(4A)CHIP#)
L3 2941 S (GROW? OR PRODUC? OR CREAT?) (8A) (NITRIDE(4A)CRYSTAL#)
L4 2821 S (HEXAGONAL) (8A) (SUBSTRATE#)
L5 156 S (CUT?) (8A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L6 197 S (GRIND?) (10A) (BACK(4A)SURFACE(10A)SUBSTRATE)
L7 1087 S (SCRATCH? OR SCRAP?) (8A) (FRONT(6A)SURFACE OR BACK(6A)SURFACE)
L8 3629 S (RHOMBUS)
L9 19827 S (SAPPHIRE(8A)SUBSTRATE)
L10 2 S L1 AND L4 AND L5
L11 5 S L1 AND L4 AND L6

=> s l1 and l4 and l5 and l6 and l7 and l8 and l9

1 FILES SEARCHED...

L12 1 L1 AND L4 AND L5 AND L6 AND L7 AND L8 AND L9

=> d l12 abs,bib

L12 ANSWER 1 OF 1 USPATFULL on STN

AB A method for manufacturing a nitride semiconductor device in which nitride crystals are sequentially grown on a substrate such as sapphire by MOCVD or the like, and p electrode and n electrode are formed. The wafer is not cut along two perpendicular directions, but rather is cut along two directions that form a 120 degree angle, to obtain a rhombus shaped semiconductor chip. Because the wafer has a six-fold rotation symmetry, by cutting the wafer at an angle of 120 degrees, the cutting directions are equivalent and the wafer can be cut in directions along which it can be easily split.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:232645 USPATFULL

TI Nitride semiconductor chip and method for manufacturing nitride semiconductor chip

IN Sakai, Shiro, Tokushima-shi, JAPAN

Lacroix, Yves, Tokushima-shi, JAPAN

PI US 2002124794 A1 20020912

AI US 2002-44686 A1 20020111 (10)

PRAI JP 2001-3910 20010111

DT Utility

FS APPLICATION

LREP ROSENTHAL & OSHA L.L.P., 1221 MCKINNEY AVENUE, SUITE 2800, HOUSTON, TX, 77010

CLMN Number of Claims: 11

ECL Exemplary Claim: 1

DRWN 4 Drawing Page(s)

LN.CNT 293

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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